AMENDMENTS TO THE SPECIFICATION

Please replace the paragraphs in the specification with the following corresponding paragraphs:

Beginning on page 1, line 24:

As a data slice circuit of the related art for separating data of a VBI signal having a CRI signal, there is known for example the circuit disclosed in Japanese Unexamined Patent Publication (Kokai) No. ~~10-336809~~10-336609.

Beginning on page 2, line 9:

FIG. 8 is a circuit diagram of the data slice circuit of the related art for separating data of a VBI signal having a CRI signal described in Japanese Unexamined Patent Publication (Kokai) No. ~~10-336809~~10-336609.

Beginning on page 4, line 20:

Also, the potential difference of the detected pedestal level Vp and the clamp level Vc is spliced at the resistors ~~R12~~ R21 and R22. The splice level Vs1 is supplied to the comparator 27. As a result, in the comparator 27, the processing for separating a synchronous signal is performed.

Beginning on page 4, line 20:

In the operational amplifier 26, the detected pedestal level Vp is input to a non-inverted input terminal (+) and the clamp level Vc is supplied to an inverted input terminal (-) via the resistor ~~R13~~R23. Then, in the operational amplifier 26, a slice level Vs2 is generated based on the pedestal level Vp, clamping level Vc, a resistance value of the resistor ~~R12~~R222, and a resistance value of a feedback resistor ~~R2~~ R24 as a slice level of the comparator 28 and this is output to the comparator 28. As a result, in the comparator 28, the processing for slicing data superposed on the input VBI signal at the vertical blanking interval etc. is performed.

Beginning on page 20, line 9:

The two input terminals of the OR circuit 3501 are connected to input lines of the window pulses PCRI and ~~PRED~~PPED, respectively, while an output terminal is connected to a gate of the NMOS transistor NT35 of the analog switch 3504 and an input terminal of the inverter 3503. An output terminal of the inverter 3503 is connected to a gate of the PMOS transistor PT35 of the analog switch 3504.

Beginning on page 25, line 16:

Similarly, the analog switch 3705 is configured by connecting sources and drains of a PMOS transistor PT372 and an NMOS transistor NT372.

Beginning on page 26, line 9:

An input terminal of the inverter 3702 is connected to the input line of the line detection pulse PLC, while an output terminal is connected to a gate of the PMOS transistor PT371 of the analog switch 3704. Also, a gate of the NMOS transistor ~~NT37~~ NT372 of the analog switch 3704 is connected to an input line of the line detection pulse PLC.

Beginning on page 28, line 7:

On the other hand, for a VBI signal having only a reference signal, the data slice level generation circuit 37 outputs a voltage value obtained by adding a specific DC voltage (Vref1-Vref0) to a pedestal level Vp as a data slice level VDSL.